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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,543	10/24/2001	Kristopher Allyn Klink	PU000147	5966

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EXAMINER	
PIZIALI, JEFFREY J	

ART UNIT	PAPER NUMBER
2673	3

DATE MAILED: 11/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,543	KLINK, KRISTOPHER ALLYN	
	Examiner	Art Unit	
	Jeff Piziali	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 8 and 9 are each objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim should refer to other claims in the alternative only. See MPEP § 608.01(n).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 6-10, 12-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Kitagawa (US 5,844,539).

Regarding claim 1, Kitagawa discloses a method of reducing a column clock [Fig. 3; VCK] time in a liquid crystal display [Fig. 1; 3] (see Column 1, Lines 5-10 and Column 4, Lines 1-22), comprising the steps of: determining if a row has all unused pixels [Figs. 2B & 2C; 32] on a row [Figs. 2B & 2C; 37]; driving all unused pixels on the row to black [Fig. 3; VBLK] simultaneously; and repeating the driving step on subsequent rows until a row with active video [Figs. 2B & 2C; 36] is detected (see Fig. 4; Column 6, Line 54 - Column 7, Line 63).

Regarding claim 2, Kitagawa discloses the unused pixels on the row or subsequent row are driven to black by applying a common DC voltage [Fig. 3; VBLK] to the row or the subsequent row (see Column 6, Lines 40-53).

Regarding claim 3, Kitagawa discloses the steps of driving all unused pixels on the row or any subsequent row comprises the steps of switching all pixels on the row or any subsequent row to a first voltage [Fig. 4; VBLK high] during the negative phase of a pixel and switching all pixels on the row or any subsequent row to a second voltage [Fig. 4; VBLK low] during a positive phase of the pixel until a row address selector reaches the active video row (see Fig. 4; Column 7, Lines 37-63).

Regarding claim 4, Kitagawa discloses the row address selector operates at a faster speed while incrementing through rows having all pixels being driven to black and operates at a slower speed while incrementing through rows having active video (see Fig. 4; Column 7, Lines 37-63).

Regarding claim 6, Kitagawa discloses the method further comprises the step of randomly accessing a start of a plurality of rows in the liquid crystal display (see Column 3, Lines 37-45). Where the row access is inherently randomly determined (note the blanked row 37 just below the display region 36 in Figs. 2B & 2C for instance) by the video signal resolution to be displayed.

Regarding claim 7, Kitagawa discloses a method of reducing a column clock [Fig. 3; VCK] time in a liquid crystal display [Fig. 1; 3] (see Column 1, Lines 5-10 and Column 4, Lines 1-22), comprising the steps of: driving all pixels [Figs. 2B & 2C; 32] on a given row [Figs. 2B & 2C; 37] to black by switching all pixels on the given row to a first voltage [Fig. 4; VBLK high] during a negative phase of a pixel until a row address selector [Fig. 3; 33] reaches an active video row [Figs. 2B & 2C; 36]; and driving all pixels on the given row to black by switching all pixels on the given row to a second voltage [Fig. 4; VBLK low] during a positive phase of the pixel until the row address selector reaches the active video row (see Fig. 4; Column 6, Line 54 - Column 7, Line 63).

Regarding claim 8, Kitagawa discloses the method further comprises the step of incrementing the row address selector and repeating the steps of claim 1 if a subsequent row has unused pixels until the address selector reaches the active video row (see Fig. 4; Column 7, Lines 37-63).

Regarding claim 9, Kitagawa discloses the method further comprises the steps of repeating the steps of claim 1 when the row address selector increments to another subsequent row having unused pixels (see Fig. 4; Column 7, Lines 37-63).

Regarding claim 10, Kitagawa discloses the row address selector operates at a faster speed while incrementing through rows having all pixels being driven to black and operates at a

slower speed while incrementing through rows having active video (see Fig. 4; Column 7, Lines 37-63).

Regarding claim 12, Kitagawa discloses the method further comprises the step of randomly accessing a start of a plurality of rows in the liquid crystal display (see Column 3, Lines 37-45). Where the row access is inherently randomly determined (note the blanked row 37 just below the display region 36 in Figs. 2B & 2C for instance) by the video signal resolution to be displayed.

Regarding claim 13, Kitagawa discloses a method of reducing a column clock [Fig. 3; VCK] time in a liquid crystal display [Fig. 1; 3] (see Column 1, Lines 5-10 and Column 4, Lines 1-22), comprising the steps of: randomly accessing a starting row in a liquid crystal display imager (see Column 3, Lines 37-45 -- where row access is inherently randomly determined by the video signal resolution to be displayed) having a plurality of rows (see Fig. 2A); and selectively addressing rows in the plurality of rows having active video [Figs. 2B & 2C; 36] and avoiding addressing rows in the plurality of rows [Figs. 2B & 2C; 37] having substantially all unused pixels [Figs. 2B & 2C; 32] (see Fig. 5; Column 7, Lines 64 - Column 8, Line 27).

Regarding claim 14, Kitagawa discloses the steps of driving all pixels on the rows having substantially all unused pixels to black by switching all pixels on the given row to a first voltage [Fig. 5; VBLK high] during a negative phase of the given pixel and switching all pixels on the

given row to a second voltage [Fig. 5; VBLK low] during a positive phase of the pixel (see Column 7, Lines 64 - Column 8, Line 27).

Regarding claim 15, Kitagawa discloses a liquid crystal display imager system [Fig. 1; 3] (see Column 1, Lines 5-10 and Column 4, Lines 1-22), comprises: an imager having a plurality of rows (see Fig. 2A) and the imager being coupled to a row address selector [Figs. 1 & 3; 33]; and a random access controller [Fig. 1; 4 working in conjunction with the SYNC signal] coupled to the row address selector that randomly accesses a row in the imager and avoids addressing rows in the imager having all unused pixels (see Fig. 5; Column 7, Lines 64 - Column 8, Line 27). Where row access is inherently randomly determined (note the blanked row 37 just below the display region 36 in Figs. 2B & 2C for instance) by the video signal resolution to be displayed.

Regarding claim 16, Kitagawa discloses the liquid crystal display imager system further comprises a switching mechanism [Fig. 3; PSW1 - PSWN] that drives all unused pixels [Figs. 2B & 2C; 32] on a given row [Figs. 2B & 2C; 37] to black simultaneously if the row in the imager has all unused pixels (see Column 6, Lines 1-53).

Regarding claim 17, Kitagawa discloses the row address selector progresses through all rows of the imager and the switching mechanism drives all unused pixels on any row having all unused pixels to black simultaneously until a row with active video [Figs. 2B & 2C; 36] is detected (see Fig. 5; Column 7, Lines 64 - Column 8, Line 27).

Regarding claim 18, Kitagawa discloses the switching mechanism drives the unused pixels on the row to black by applying a common DC voltage [Fig. 3; VBLK] to the row (see Column 6, Lines 40-53)

Regarding claim 19, Kitagawa discloses the switching mechanism switches all pixels on the row having all unused pixels to a first voltage [Fig. 5; VBLK high] during the negative phase of a pixel and switches all pixels on the row having all unused pixels to a second voltage [Fig. 5; VBLK low] during a positive phase of the pixel until the row address selector reaches an active video row (see Column 7, Lines 64 - Column 8, Line 27).

Regarding claim 20, Kitagawa discloses the row address selector operates at a faster speed while incrementing through rows having all pixels being driven to black and operates at a slower speed while incrementing through rows having active video (see Fig. 4; Column 7, Lines 37-63).

Regarding claim 21, Kitagawa discloses the system further comprises a sample and hold circuit [Fig. 1; 1 & 2 operating in conjunction] coupled to the random access controller [Fig. 1; 4 working in conjunction with the SYNC signal] to enable the random access controller to detect rows [Figs. 2B & 2C; 37] having all unused pixels [Figs. 2B & 2C; 32] (see Column 4, Lines 58).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitagawa (US 5,844,539) in view of Fairbanks et al. (US 5,130,703).

Regarding claims 5 and 11, Kitagawa does not explicitly disclose the first voltage is 16 volts and the second voltage is 0 volts. However, Fairbanks does disclose driving a liquid crystal display (see Column 1, Lines 5-10) with a first voltage of 16 volts and a second voltage of 0 volts (see Column 3, Line 61 - Column 4, Line 9). Kitagawa and Fairbanks are analogous art, because they are from the shared field of driving liquid crystal display devices. Therefore, it would have been obvious to one skilled in the art at the time of invention to use Fairbanks' voltage levels with Kitagawa's clock time reduction method and circuitry, so as to optimize screen contrast and picture quality.

6. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitagawa (US 5,844,539) in view of Huang et al. (US 5,965,907).

Regarding claim 22, Kitagawa does not explicitly disclose the system is for a liquid crystal on silicon crystal display. However, Huang does disclose substituting an active matrix LCD with a liquid crystal on silicon crystal display (see Column 4, Lines 46-67). Kitagawa and Huang are analogous art, because they are from the shared field of liquid crystal display devices.

Therefore, it would have been obvious to one skilled in the art at the time of invention to use Huang's LCoS display as Kitagawa's LCD, so as to utilize a display that is relatively easy and inexpensive to manufacture.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Zenda (US 4,990,902), Rabii (US 5,159,438), Ezaki (US 5,416,598), Nishikawa (US 5,592,194), Shin (US 5,781,185), Sharp et al. (US 5,929,946), Ogawa (US 6,018,331), Park et al. (US 6,362,804), and Singla et al. (US 6,597,373) are cited to further evidence the state of the art pertaining to liquid crystal displays.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

J.P.
12 November 2003

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